Patent claims

1. Method for filling a contact hole (20), in which a base layer (50) is deposited in at least one contact hole (20) under a protective gas, which base layer contains a nitride as main constituent and keeps gaseous nitrogen away from the bottom (24) of the contact hole (20), and in which a covering layer (54) is deposited in the contact hole (20) after the deposition of the base layer (50) under gaseous nitrogen, which covering layer contains a nitride as main constituent.

2. Method according to Claim 1, characterized in that the base layer (50) and/or the covering layer (54) is deposited by directional sputtering.

3. Method according to Claim 1 or 2, characterized in that an intermediate layer (52) is deposited in the contact hole (20) after the deposition of the base layer (50) and before the deposition of the covering layer (54) preferably by directional sputtering, which intermediate layer contains a nitride-free main constituent.

4. Method according to Claim 3, characterized in that at least one region (B3, B4) of the intermediate layer (52) is deposited from a nitride-free surface of a sputtering target (108) under a protective gas.

5. Method according to one of Claims 2 to 4, characterized in that the surface (157) of the sputtering target, for the sputtering of the base layer (50), is nitrided before the deposition of the base layer (50) under nitrogen.

6. Method according to one of Claims 2 to 5, characterized in that the base layer (50) and the covering layer (54) and preferably also the intermediate layer (52) are produced using the same sputtering target (108).

7. Method according to one of the preceding claims, characterized in that the contact hole (20) is introduced into a dielectric layer (18) as far as an electrically conductive connecting section (14),
and in that the connecting section (14) preferably contains aluminium or an aluminium alloy as main constituent.

8. Method according to Claim 7, characterized in that a multiplicity of contact holes (20) are etched simultaneously into the dielectric layer (18),
in that an electrically conductive auxiliary layer (16), preferably an antireflection layer, is arranged between the dielectric carrier material (18) and the connecting section (14),
and in that the auxiliary layer (16) is used as a stop layer during the etching, a penetration of the auxiliary layer (16) at thin locations of the dielectric layer and/or at locations with a higher etching rate being accepted, however.

9. Method according to one of the preceding claims, characterized in that a contact hole filling is deposited in the contact hole (20) after the deposition of the covering layer (54) preferably under tungsten hexafluoride, which contact hole filling contains tungsten as main constituent.

10. Method according to one of the preceding claims, characterized in that the base layer (50) together with the intermediate layer (52), at the bottom

(24) of the contact hole, has a thickness (D2, D3) of less than 5 nm, in particular less than 3 nm, and/or in that the covering layer (54), at the bottom (24) of the contact hole, has a thickness (D4) of less than 20 nm, preferably less than 10 nm.

11. Method according to one of the preceding claims, characterized in that the contact hole (20) has a diameter of less than 1 µm, preferably of about 0.5 µm,
and/or in that the contact hole (20) has a depth of greater than 500 nm, preferably greater than 1 µm.

12. Method according to one of the preceding claims, characterized in that the base layer (50) and/or covering layer (54) contains titanium nitride or tantalum nitride as main constituent,
and/or in that the intermediate layer (52) contains titanium or tantalum as main constituent.

13. Integrated circuit arrangement (10),
having at least one contact hole (20), in which a base layer (50) and a covering layer (54) are arranged,
the base layer (50) containing, as main constituent, a nitride which has been deposited under a protective gas,
and the covering layer (54) containing, as main constituent, a nitride which has been deposited under gaseous nitrogen.

14. Circuit arrangement (10) according to Claim 13, characterized by an intermediate layer (52) arranged between the base layer (50) and the covering layer (54) which intermediate layer contains a nitride-free main constituent.

15. Circuit arrangement (10) according to Claim 13 or 14, characterized in that the circuit arrangement (10) has been produced by a method according to one of Claims 1 to 12.